A2D CONVERTORS + PIC24 TIMING

This chapter covers analog-to-digital (A/D) and digital-to-analog (D/A) conversion. We will learn how to specify a converter for a particular application and how a variety of A/Ds and D/As work.

CADY

13.2 Data Acquisition and Conversion

Figure 13-1 shows a *data acquisition system* to input analog data. It receives analog information from a physical variable, such as temperature, and uses a *transducer* to convert the information to an electrical signal, either voltage or current. Following the transducer is a block labeled *signal conditioning* to provide the following functions:

Amplification: Rarely does the transducer produce the voltage or current needed by the A/D. The amplifier is designed so that the full-scale signal from the analog input results in a full-scale signal to the A/D.

Bandwidth limiting: The signal conditioning provides a low-pass filter to limit the range of frequencies that can be digitized. To understand why this is so, we will consider the sampling theorem and learn about aliasing in Section 13.3.

Isolation and buffering: The input to the A/D may need to be protected from dangerous voltages such as static discharges or reversed polarity voltages.

An *analog multiplexer* follows the signal conditioning in applications that call for the digitization of several analog inputs. This computer-controlled switch allows multiple analog inputs, each with its own signal conditioning for different transducers, to be switched into a single A/D. The CPU generates an address on the multiplexer select lines to select the multiplexer channel.

Data Acquisition System Operation

The operation of the system shown in Figure 13-1 can be described as follows.

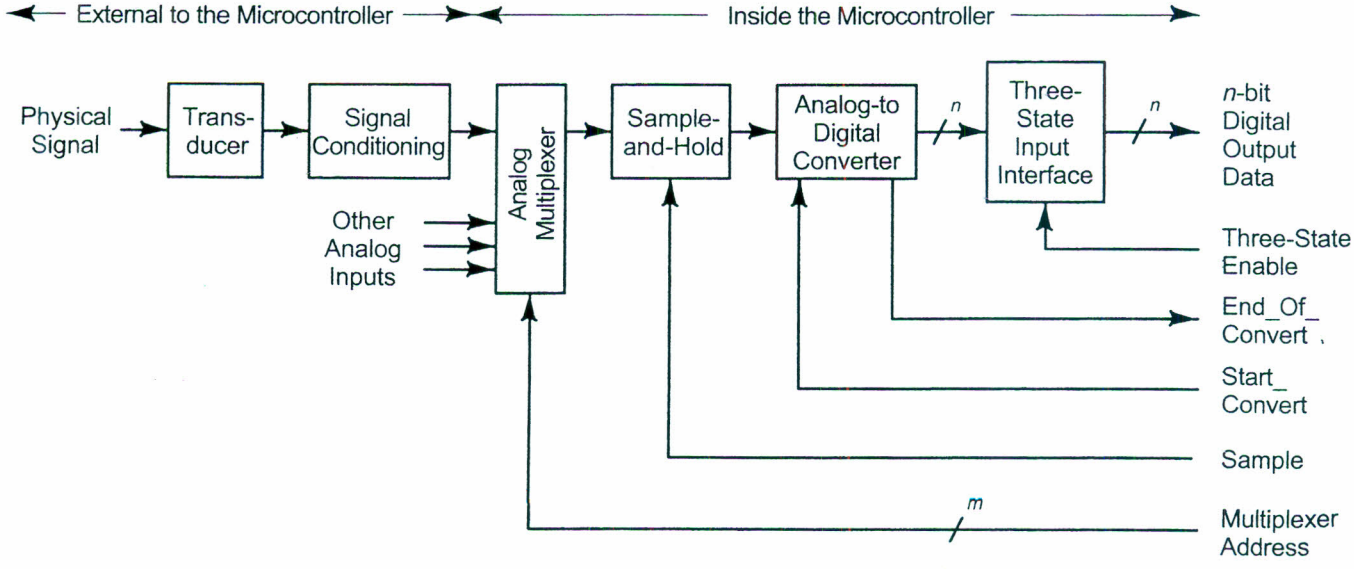


Figure 13-1 Data acquisition system.

- The program selects the analog signal to be digitized by outputting an address to the analog multiplexer.
- As we will discuss shortly, a sample-and-hold circuit may be needed to hold the analog signal constant while the analog-to-digital converter is working. In such cases, the program asserts the *sample* signal to take a quick snapshot of the analog signal.
- Following the sample-and-hold action, the program asserts the *Start_Convert* signal to start the A/D.
- When the A/D finishes the conversion, it asserts the *End_Of_Convert* signal, which allows the program to input the data through the three-state input interface.

Definitions

Let us define some of the terms you will encounter as you learn about the analog-to-digital conversion. We begin with a fundamental concept and illustrate it in Example 13-1.

Resolution: The resolution is the smallest change in the input analog signal that will produce a change in the output digital code:

$$V_{\text{resolution}} = \frac{V_{\text{full-scale value}}}{2^n} \text{ VOLTS}$$

Resolution is also stated in terms of the number of bits in the output digital code, or as one part in 2^n. Sometimes the resolution is given as a percentage of maximum or full-scale value:

$$V_{\text{resolution}} = \frac{1}{2^n} \times 100\% \text{ of full-scale value}$$

Example 13-1 A/D Resolution

An 8-bit A/D converter is to digitize a 5 volt, full-scale signal. What is the resolution?

Solution

The resolution is 5/256 = 19.5 mV. Another way of stating the resolution is 1 part in 256, or 0.4% of the full-scale value. $1/256 \times 100\% = 0.390625\%$

Additional definitions follow.

Accuracy: Accuracy is often confused with resolution. Resolution relates the smallest signal (or noise) to the full-scale value. Accuracy relates the smallest signal to the measured signal.

Accuracy is given as a percentage and describes how close the measurement is to the actual value. We say the digital representation of our signal is accurate to within

$$\frac{V_{\text{resolution}}}{V_{\text{signal}}} \times 100\%$$

$2^8 = 256$

See Example 13-2.

A/D transfer function: The A/D transfer function shows the digital output code as a function of the input voltage. Figure 13-2 shows a transfer function for a 3-bit A/D. As the voltage increases from zero, the output code steps up one bit at a time, ranging from 000 to 111.

Example 13-2 A/D Accuracy

An 8-bit A/D converter digitizes a 5-volt, full-scale signal. What is the accuracy with which the A/D can digitize the following signals?
50 mV, 1 V, 2.5 V, 4.9 V

Solution

The resolution is 5 V/256 = 19.5 mV. Each measurement will be accurate to within the listed percentage value:

50 mV	(19.5 mV/50 mV) = 39%
1 V	(19.5 mV/1 V) = 1.9%
2.5 V	(19.5 mV/2.5 V) = 0.8%
4.9 V	(19.5 mV/4.9 V) = 0.4%

Aperture time: This is the time that the A/D converter is looking at the input signal. It is usually equal to the conversion time. We will see in the next section how any change in the input signal during this time may cause an error in the output code.

Conversion time: The conversion time is the time required to complete a conversion of the input signal. It establishes the upper signal frequency limit that can be sampled without aliasing:

$$f_{\max} = \frac{1}{2 \times \text{conversion time}}$$

Ex $T_S = 10^{-3}$ s

$f_{max} = \frac{1}{2 \times 10^{-3}} = 500$ Hz

Dynamic range: The dynamic range of a signal is the ratio of the maximum signal to the smallest, or noise level, signal.

$$\text{Dynamic range} = \frac{V_{\max}}{V_{\text{noise}}}$$

$\frac{V_{max}}{V_{min}} = 2^N$

$N = \log_2\left(\frac{V_{max}}{V_{min}}\right)$

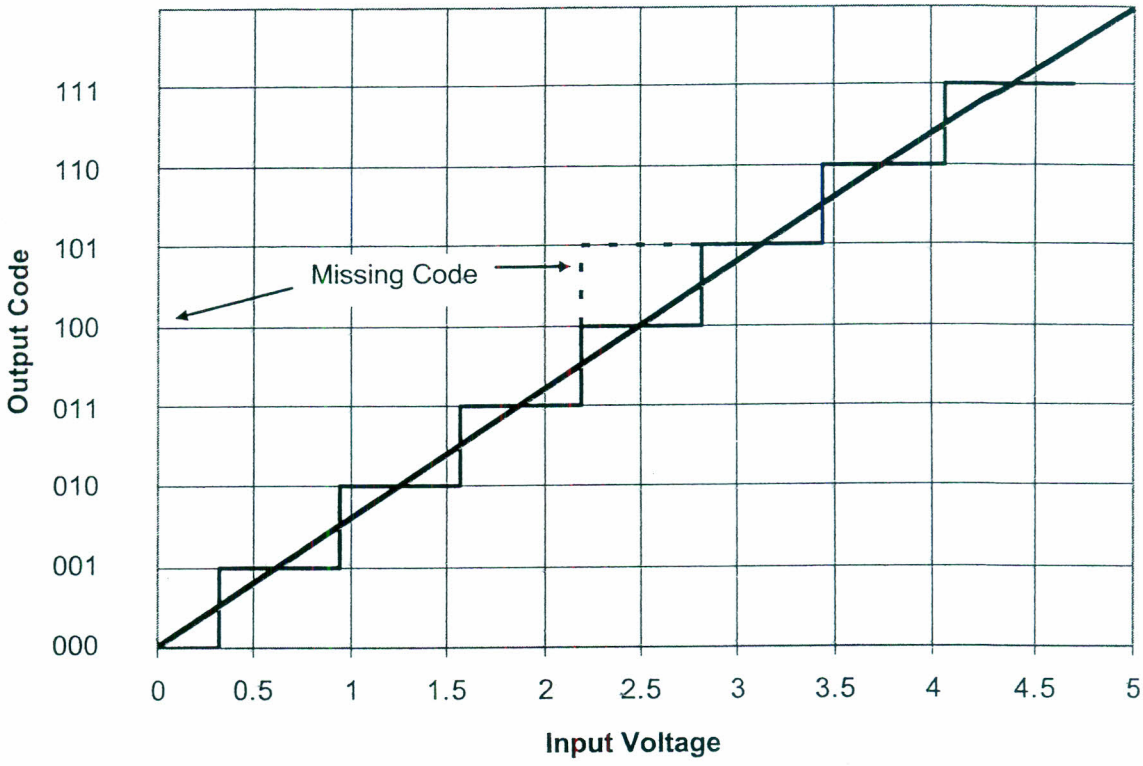


Figure 13-2 A 3-bit A/D transfer function.

Dynamic range may also be stated in decibels.

$$\text{Dynamic range} = 20 \log_{10} \frac{V_{max}}{V_{noise}} \text{ dB}$$

Linearity: Linearity is the deviation in output codes from a straight line drawn through zero and full scale. The best that can be achieved is ±0.5 of the least significant bit (±0.5LSB), as shown in Figure 13-2.

Missing codes: The transfer function for a converter with a missing code is shown in Figure 13-2. An internal error might be the cause of a missing code.

13.3 Shannon's Sampling Theorem and Aliasing

The frequency at which signals are sampled must be at least two times the highest frequency in the signal.

Claude Shannon showed that when a signal, $f(t) = X \sin 2\pi f_{sig} t$, is to be sampled (digitized), the *minimum sampling frequency must be twice the signal frequency.*[1] Consider the waveform in Figure 13-3 whose frequency is f_{sig}. When the sampling frequency f_{sample}, is twice f_{sig}, the waveform is sampled at points A and B. The problem we now pose, and

[1] C. E. Shannon, "A Mathematical Theory of Communication," *Bell Sys. Tech. J.*, vol. 27, 1948, pp. 379–423.

13.5 Choosing the A/D Converter

The designer must choose the number of bits, or resolution, and the speed, or conversion time, of the converter. The type of digital code output from the converter may be chosen. The aperture time must be calculated and a decision made to include a sample-and-hold and an antialiasing filter in the system.

Choosing the A/D Resolution

There are two ways to find the resolution needed in the A/D. The first is to find the dynamic range of the input signal and to choose the number of bits based on this. The *dynamic range* of any signal is given by

$$\text{Dynamic range} = \frac{V_{max}}{V_{noise}}$$

where V_{max} is the maximum input signal and V_{noise} is the noise. We would like the noise to be within ± 0.5 LSB, as shown in Figure 13-7, and for this to be true, the number of bits is

$$N \geq \log_2 \frac{V_{max}}{V_{noise}}$$

This is the best one can do unless signal processing, such as averaging, can reduce the noise.

Another way to choose the number of bits is based on the resolution required in the signal. Here, V_{min} is the required resolution, and it determines the number of bits by means of the following relation (see Example 13-5):

$$N \geq \log_2 \frac{V_{max}}{V_{min}}$$

Example 13-5 Choosing the A/D Resolution

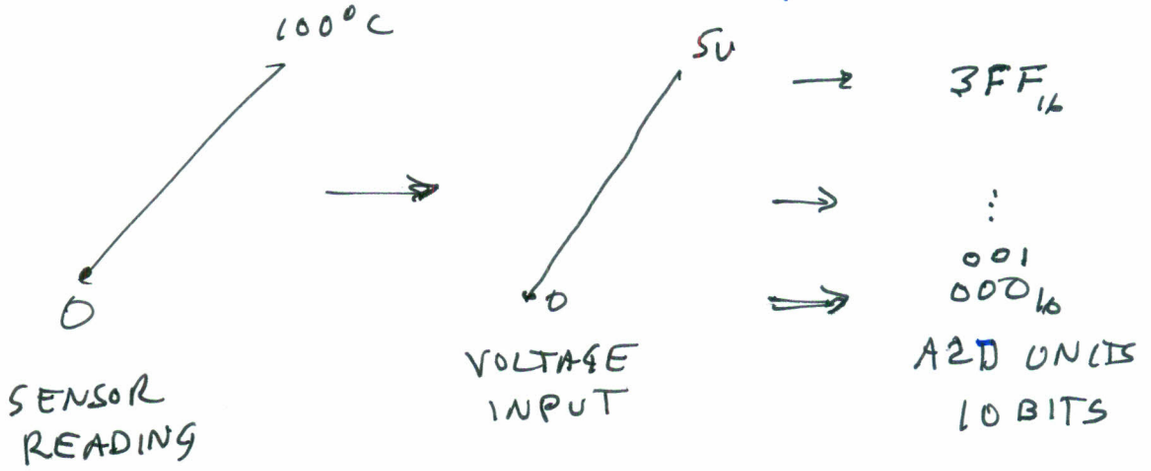
A transducer is to be used to find the temperature over a range of zero to 100°C. We are required to read and display the temperature to a resolution of ±1°C. The transducer produces a voltage from 0 to 5 V over this temperature range with 5 MV of noise. Specify the number of bits in the A/D converter (a) based on the dynamic range of the signal and (b) based on the required resolution.

Solution

(a) The dynamic range is (5 V)/(0.005 V) = 1000. Thus a 10-bit A/D converter is required if the noise is to be < ±0.5 LSB.

(b) The required resolution is 1°C in 100°C, or 100:1. A 7-bit converter will meet these specifications. In practice, an 8-bit converter would be chosen in a microcontroller-based system. The least significant bit can be thrown away or used for signal processing.

P 320 EXAMPLE 13-5 CADY



So $V_{sensor/°C} = \frac{5V}{100°C} = 0.05\,V/°C$

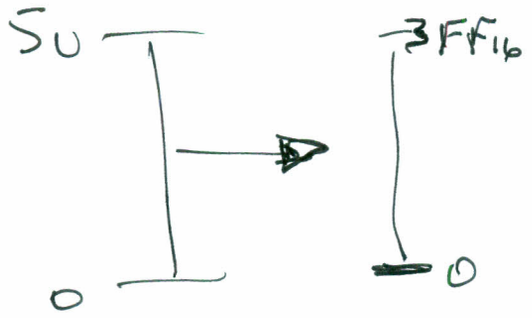
So $V_{sensor} = 0.05V/°C \times T°C$

$V_{senson} = 0.05V$ at $1°C$ (50mV)

THE 10 bit RESOLUTION IS $\frac{5V}{2^{10}} = 4.88mV$ ✓

$V_{sensor\ max} = 0.05V/°C \times 100°C = 5$ VOLTS ✓

ASSUME LINEAR



$$\frac{X_V}{5V} = \frac{Y_{16}}{3FF_{16}}$$

$$Y_{16} = 3FF \times \frac{X_V}{5}$$

So $Y_{16} = 3FF \cdot \frac{2.5}{5}$ at 2.5V

$$= \frac{3FF}{2} = 1FF_{16} \; (511_{10}) \checkmark$$

MATLAB CHECK

hex2dec('1FF') = 511_{10}

$$Y_{16} = 3FF \cdot \left[\frac{5 \times 10^{-3}}{5}\right]$$ ONE COUNT

OR ONE COUNT $= \frac{5V}{1024} = 0.0049V \approx 4.9mV$

OR ONE COUNT $\doteq \frac{1}{10}\,^{0}C$

(2) CHOOSE SAMPLING TIME AND DURATION

HARMAN

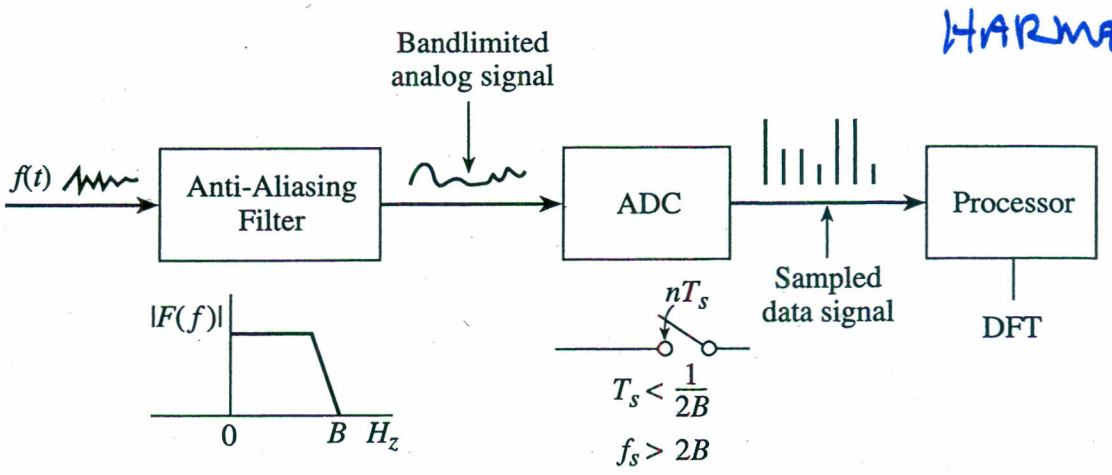


FIGURE 11.7 *Data acquisition system (repeated for convenient reference)*

The signal will be assumed to be a *continuous-time* signal, which is often referred to as an *analog* signal. A system that converts the analog signal to a sequence of time samples suitable for computer processing is called a *data acquisition system*. The first component is a filter that eliminates unwanted frequency components of a signal. In this case, the filter limits the frequencies in the signal to the range 0 to B. A signal filtered in this way is said to be *bandlimited* to B hertz. In a data acquisition system, the filter is sometimes called a *presampling filter*. Such a filter is also called an *anti-aliasing* filter because it is intended to prevent an error called aliasing, as explained later after the sampling theorem is presented.

The analog-to-digital converter (ADC) samples the filtered signal each T_s seconds to create a *sampled-data* or *digital* signal, which is the discrete-time representation of the analog signal after sampling. Typically, the samples are stored in a computer's memory for processing.

SAMPLING

Two of the most important questions in the specification of a data acquisition system such as that shown in Figure 11.7 are the following:

1. How often should the analog signal be sampled? - MAX FREQUENCY
2. How long should the signal be sampled? - RESOLUTION IN FREQUENCY

If the highest frequency of interest in the signal is B hertz and the frequency spectrum of the signal is limited to B hertz by the anti-aliasing filter, the *sampling theorem* answers the question in Part 1. The theorem is the cornerstone of practical and theoretical studies in electronic communication.

Sampling Theorem Suppose the highest frequency contained in an analog signal $f(t)$ is $f_{\max} = B$ hertz. Then, if $f(t)$ is sampled periodically

at a rate of

$$f_{\text{sample}} = 1/T_s > 2B \tag{11.10}$$

samples per second, the signal can be exactly recovered from the sample values.[2]

Considering the sampling interval T_s, the sampling theorem states that the analog signal must be sampled so that more than two samples per cycle of the highest frequency in the signal are taken. Since a cycle of the sinusoid at B hertz is $1/B$ seconds in length, the sampling interval must be less than $1/(2B)$ seconds, as indicated in the sampling theorem. The frequency $2B$ is called the *Nyquist frequency*, and the corresponding sampling rate is the *Nyquist rate*. Thus, an analog signal must be sampled at a rate greater than the Nyquist rate if errors due to sampling at too low a rate are to be avoided.

For example, if the signal contains frequencies up to $B = 1000$ hertz, the Nyquist frequency is 2000 hertz and the sampling theorem requires sampling at a rate higher than 2000 samples per second. In terms of the parameters defined earlier for the DFT, the sampling interval corresponding to the Nyquist rate must be

$$T_s < \frac{1}{2B} = \frac{1}{2000} \quad \text{seconds},$$

or $T_s < 0.5$ milliseconds, between samples. Another way to view this is to realize that a 1000-hertz sinusoid repeats every millisecond. Sampling more than two samples per cycle requires a sampling interval of less than $1/(2 \times 10^3)$ seconds. The length of time the signal is sampled would be $(N-1)T_s$ seconds if N samples are taken.

Sampling and the DFT Suppose that an analog signal is sampled at a rate

$$f_{\text{sample}} = \frac{1}{T_s} > 2B \quad \text{samples/second}.$$

The highest possible frequency in the DFT spectrum would be $F_{\max} = 1/(2T_s)$ hertz. If the signal is bandlimited to B hertz and sampled properly, the component at the DFT maximum frequency should be zero since $F_{\max} > B$ hertz.

Although the sampling theorem gives an elegant solution to the sampling problem, a number of practical considerations intervene to complicate the selection of a sampling rate. First, the reader should review the examples in this chapter and in Chapter 8 and notice that none of the ideal example signals have a bandlimited spectrum. In practice, this is not a problem because any physical signal is in fact bandlimited. The physical system that created the signal cannot oscillate above some finite frequency, and the energy content of the signal is negligible beyond

[2]The interpolation function to reconstruct the analog signal is discussed in most textbooks that cover digital signal processing. Several of these books are listed in the Annotated Bibliography at the end of this chapter.

PIC 24 A2D TIMING

PIC24FV32KA304 FAMILY

20/28/44/48-Pin, General Purpose, 16-Bit Flash Microcontrollers with XLP Technology

Power Management Modes:

- Run – CPU, Flash, SRAM and Peripherals On
- Doze – CPU Clock Runs Slower than Peripherals
- Idle – CPU Off, Flash, SRAM and Peripherals On
- Sleep – CPU, Flash and Peripherals Off and SRAM on
- Deep Sleep – CPU, Flash, SRAM and Most Peripherals Off; Multiple Autonomous Wake-up Sources
- Low-Power Consumption:
  - Run mode currents down to 8 µA, typical
  - Idle mode currents down to 2.2 µA, typical
  - Deep Sleep mode currents down to 20 nA, typical
  - Real-Time Clock/Calendar currents down to 700 nA, 32 kHz, 1.8V
  - Watchdog Timer 500 nA, 1.8V typical

High-Performance CPU:

- Modified Harvard Architecture
- Up to 16 MIPS Operation @ 32 MHz
- 8 MHz Internal Oscillator with 4x PLL Option and Multiple Divide Options
- 17-Bit by 17-Bit Single-Cycle Hardware Multiplier
- 32-Bit by 16-Bit Hardware Divider 16-Bit x 16-Bit Working Register Array
- C Compiler Optimized Instruction Set Architecture

Peripheral Features:

- Hardware Real-Time Clock and Calendar (RTCC):
  - Provides clock, calendar and alarm functions
  - Can run in Deep Sleep mode
  - Can use 50/60 Hz power line input as clock source
- Programmable 32-bit Cyclic Redundancy Check (CRC)
- Multiple Serial Communication modules:
  - Two 3-/4-wire SPI modules
  - Two I^2C™ modules with multi-master/slave support
  - Two UART modules supporting RS-485, RS-232, LIN/J2602, IrDA®
- Five 16-Bit Timers/Counters with Programmable Prescaler:
  - Can be paired as 32-bit timers/counters
- Three 16-Bit Capture Inputs with Dedicated Timers
- Three 16-Bit Compare/PWM Output with Dedicated Timers
- Configurable Open-Drain Outputs on Digital I/O Pins
- Up to Three External Interrupt Sources

Analog Features:

10 µs

- 12-Bit, up to 16-Channel Analog-to-Digital Converter:
  - 100 ksps conversion rate
  - Conversion available during Sleep and Idle
  - Auto-sampling timer-based option for Sleep and Idle modes
  - Wake on auto-compare option
- Dual Rail-to-Rail Analog Comparators with Programmable Input/Output Configuration
- On-Chip Voltage Reference
- Internal Temperature Sensor
- Charge Time Measurement Unit (CTMU):
  - Used for capacitance sensing, 16 channels
  - Time measurement, down to 200 ps resolution
  - Delay/pulse generation, down to 1 ns resolution

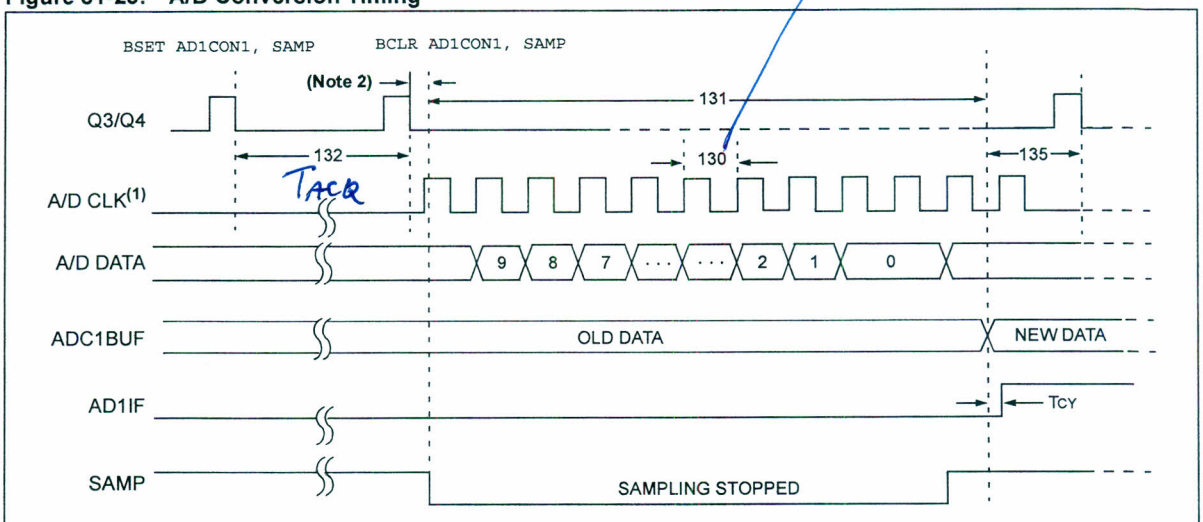
* some models have 10 bit Resolution

Special Microcontroller Features:

- Wide Operating Voltage Range:
  - 1.8V to 3.6V (PIC24F devices)
  - 2.0V to 5.5V (PIC24FV devices)
- Low Power Wake-up Sources and Supervisors:
  - Ultra-Low Power Wake-up (ULPWU) for Sleep/Deep Sleep
  - Low-Power Watchdog Timer (DSWDT) for Deep Sleep
  - Extreme Low-Power Brown-out Reset (DSBOR) for Deep Sleep, LPBOR for all other modes
- System Frequency Range Declaration bits:
  - Declaring the frequency range optimizes the current consumption.
- Standard Watchdog Timer (WDT) with On-Chip, Low-Power RC Oscillator for Reliable Operation
- Programmable High/Low-Voltage Detect (HLVD)
- Standard Brown-out Reset (BOR) with 3 Programmable Trip Points that can be Disabled in Sleep
- High-Current Sink/Source (18 mA/18 mA) on All I/O Pins
- Flash Program Memory:
  - Erase/write cycles: 10,000 minimum
  - 40 years' data retention minimum
- Data EEPROM:
  - Erase/write cycles: 100,000 minimum
  - 40 years' data retention minimum
- Fail-Safe Clock Monitor
- Programmable Reference Clock Output
- Self-Programmable under Software Control
- In-Circuit Serial Programming™ (ICSP™) and In-Circuit Debug (ICD) via 2 Pins

51.17 ELECTRICAL SPECIFICATIONS

Figure 51-23: A/D Conversion Timing



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

2: This is a minimal RC delay (typically 100 ns) which also disconnects the holding capacitor from the analog input.

Table 51-7: A/D Conversion Requirements

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
AD61	tPSS	Sample Start Delay from Setting SAMP	2	—	3	TAD	
AD130	TAD	A/D Clock Period	75	—	—	ns	TOSC-based
			—	250	—	ns	A/D RC mode
AD131	TCNV	Conversion Time (not including acquisition time)	11	—	12	TAD	**(Note 1)**
AD132	TACQ	Acquisition Time	—	—	750	ns	**(Note 2)**
AD135	TSWC	Switching Time from Convert to Sample	—	—	**(Note 3)**		
AD137	TDIS	Discharge Time	0.5	—	—	TAD	
		A/D Stabilization Time (from setting ADON to setting SAMP)	—	300	—	ns	

Note 1: The ADC1BUF register may be read on the following TCY cycle.

2: The time for the holding capacitor to acquire the "New" input voltage when the voltage changes full scale after the conversion (AVDD to AVSS or AVSS to AVDD).

3: On the following cycle of the device clock.

EXAMPLE

$T_{ACQ} = 750ns$

$T_{A/D} = 250ns$

Page 51 ADD 132 + 131

$T_{ACQ} + N * T_{AD}$; $N = 12$

$T_{min} = 750ns + 12 \times 250ns$

$= 750ns + 3000ns$

$= 3750ns = 3.75\mu s$

So $S_{max} = \frac{1}{3.75 \times 10^{-6} s} = 266,666$ samples/sec

$f_{max} = \frac{1}{2} S_{max} = 133,333$ Hz for FFT.

NOTE: IN PRACTICE, ADD SOFTWARE TIME

START A/D ; MOVE DATA FROM ADBUFFER TO MEMORY

SO TEST ROUTINE TO SEE MAXIMUM SPEED