I/O Ports with Peripheral Pin Select (PPS)

HIGHLIGHTS

This section of the manual contains the following topics:

dsPIC33/PIC24 Family Reference Manual

> **Note:** This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33/PIC24 devices.
>
> Please consult the note at the beginning of the **"I/O Ports"** chapter in the current device data sheet to check whether this document supports the device you are using.
>
> Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Website at: http://www.microchip.com

1.0   INTRODUCTION

The general purpose I/O pins can be considered the simplest of peripherals. They allow the PIC® MCU to monitor and control other devices. To add flexibility and functionality to a device, some pins are multiplexed with alternate function(s). These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

Most of the dsPIC33/PIC24 devices support the Peripheral Pin Select (PPS) feature. The PPS constitutes pins which users can map to the input and/or output of some digital peripherals.

Figure 1-1 shows a block diagram of a typical I/O port. This block diagram does not take into account peripheral functions that may be multiplexed onto the I/O pin.

Figure 1-1:   **Dedicated Port Structure Block Diagram**
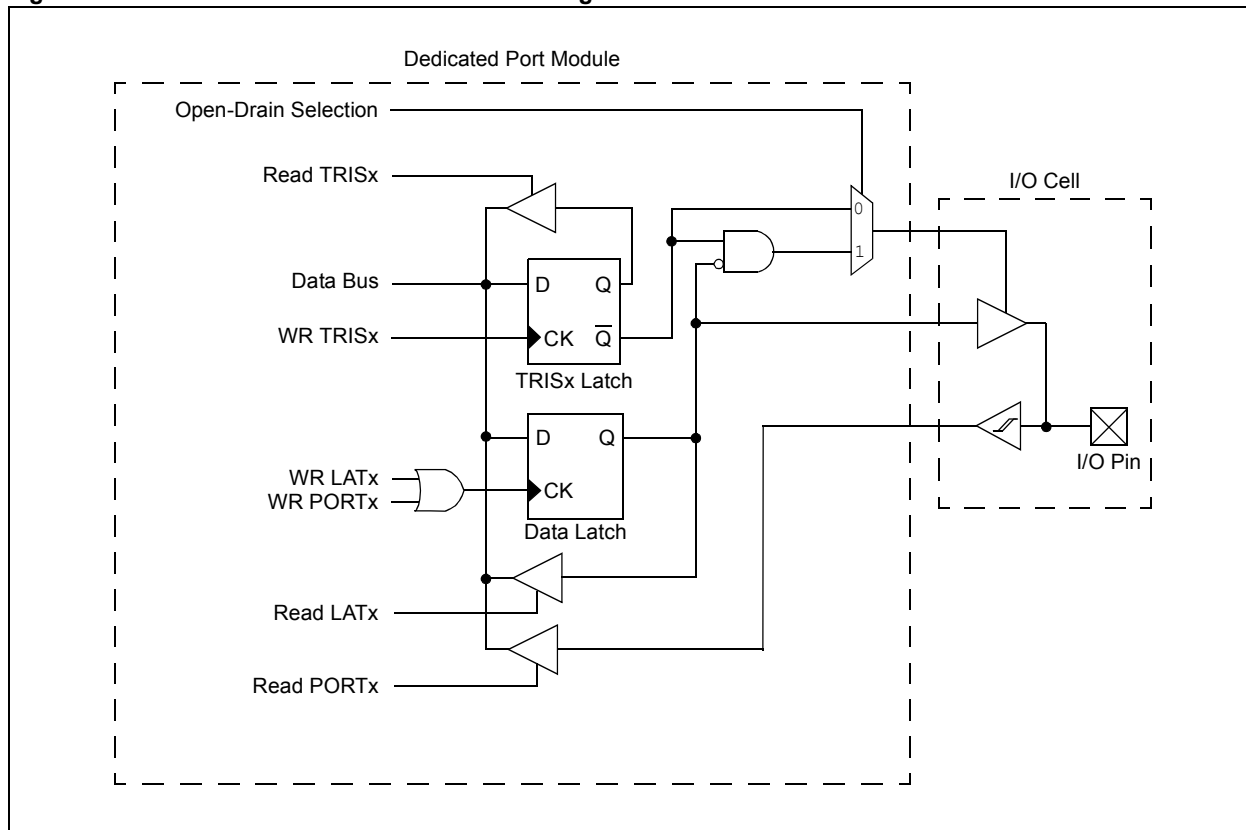
2.0   I/O PORT CONTROL REGISTERS

All I/O ports have four registers directly associated with the operation of the port, where 'x' is a letter that denotes the particular I/O port:

- TRISx: PORTx Data Direction Control register
- PORTx: I/O Portx register
- LATx: PORTx Data Latch register
- ODCx: PORTx Open-Drain Control register

Each I/O pin on the device has an associated bit in the TRISx, PORTx, LATx and ODCx registers.

> **Note:**   The total number of ports and available I/O pins will depend on the device variant. In a given device, all of the bits in a PORT register may not be implemented. Refer to the specific device data sheet for further details.

2.1   TRIS Registers

The TRISx register control bits determine whether each pin associated with the I/O port is an input or an output. If the TRISx bit for an I/O pin is a '1', then the pin is an input. If the TRISx bit for an I/O pin is a '0', then the pin is configured as an output. An easy way to remember this is that a '1' looks like an I (Input) and a '0' looks like an O (Output). All port pins are defined as inputs after a Reset.

> **Note:**   Set the pin as an output and drive to zero (TRISx = 1, LATx = 1) prior to making the I/O pin an input (TRISx = 1). This helps discharge the parasitic capacitance internal to the I/O pin.
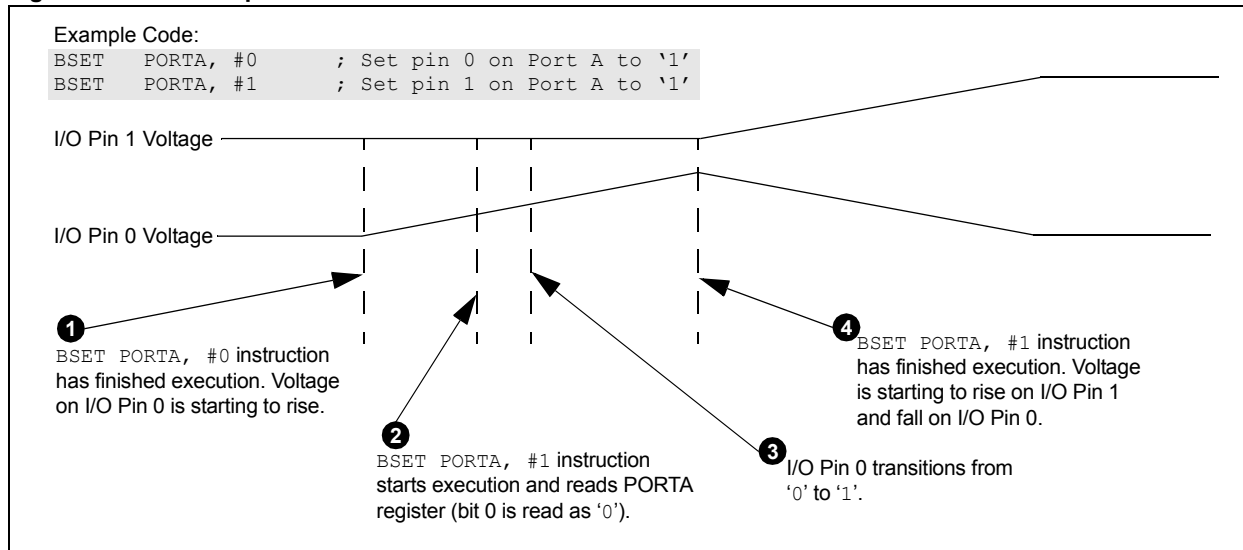
2.2   PORT Registers

Data on an I/O pin are accessed via a PORTx register. A read of the PORTx register reads the value of the I/O pin, while a write to the PORTx register writes the value to the port data latch. This will also be reflected on the PORTx pins if the TRISx is configured as an output and the multiplexed peripherals (if any) are disabled.

Many instructions, such as BSET and BCLR, are Read-Modify-Write (RMW) operations. Therefore, a write to a port implies that the port pins are read, the value is modified and then written back to the port data latch. Care should be taken when Read-Modify-Write instructions are used on the PORTx registers when some I/O pins associated with the port are configured as inputs. If an I/O pin configured as an input is changed to an output, at some later time, an unexpected value may be output on the I/O pin. To avoid this, first write to the associated PORTx bit and then change the direction of the pin as an output.

In addition, if Read-Modify-Write instructions are used on the PORTx registers while I/O pins are configured as outputs, unintended I/O behavior may occur based on the device speed and I/O capacitive loading. Figure 2-1 illustrates unintended behavior that occurs if the user application attempts to set I/O bits, 0 and 1 on PORTA, with two consecutive Read-Modify-Write instructions in the PORTA register. At high CPU speeds and high-capacitive loading on the I/O pins, the unintended result of the example code is that only I/O bit 1 is set high.

Figure 2-1: **Example of Unintended I/O Behavior**

```
Example Code:
BSET    PORTA, #0       ; Set pin 0 on Port A to '1'
BSET    PORTA, #1       ; Set pin 1 on Port A to '1'
```

I/O Pin 1 Voltage

I/O Pin 0 Voltage

① `BSET PORTA, #0` instruction has finished execution. Voltage on I/O Pin 0 is starting to rise.

② `BSET PORTA, #1` instruction starts execution and reads PORTA register (bit 0 is read as '0').

③ I/O Pin 0 transitions from '0' to '1'.

④ `BSET PORTA, #1` instruction has finished execution. Voltage is starting to rise on I/O Pin 1 and fall on I/O Pin 0.

2.3 LAT Registers

The LATx register associated with an I/O pin eliminates the problems that could occur with Read-Modify-Write instructions. A read of the LATx register returns the values held in the port output latches instead of the values on the I/O pins. A Read-Modify-Write operation on the LATx register, associated with an I/O port, avoids the possibility of writing the input pin values into the port latches. A write to the LATx register has the same effect as a write to the PORTx register.

The differences between the PORTx and LATx registers can be summarized as follows:

• A write to the PORTx register writes the data value to the port latch.
• A write to the LATx register writes the data value to the port latch.
• A read of the PORTx register reads the data value on the I/O pin.
• A read of the LATx register reads the data value held in the port latch.

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers, and the port pin, will read as zeros.

2.4 ODC Registers

Each I/O pin can be individually configured for either normal digital output or open-drain output. This is controlled by the PORTx Open-Drain Control register, ODCx, associated with each I/O pin. If the ODC bit for an I/O pin is '1', then the pin acts as an open-drain output. If the ODC bit for an I/O pin is '0', then the pin is configured for a normal digital output (ODC bit is valid only for output pins). After a Reset, the status of all the bits of the ODCx register is set to '0'.

The open-drain feature allows a load to be connected to a voltage higher/lower than V_{DD} on any desired digital only pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum V_{IH} specification and the minimum is V_{SS}. The ODCx register setting takes effect in all the I/O modes, allowing the output to behave as an open-drain, even if a peripheral is controlling the pin. Although the user could achieve the same effect by manipulating the corresponding LAT and TRIS bits, this procedure will not allow the peripheral to operate in Open-Drain mode (except for the default operation of the I^{2}C pins). Since I^{2}C pins are already open-drain pins, the ODCx settings do not affect the I^{2}C pins. Also, the ODCx settings do not affect the JTAG output characteristics as the JTAG scan cells are inserted between the ODCx logic and the I/O.

Note:	Please note that the maximum V_{IH} spec for the PIC24FXXKXXXX family is limited to V_{DD}. This limits open-drain capability for higher voltage generation, though it can still be connected to lower voltage than V_{DD}.

Register 2-1:   TRISx: PORTx Data Direction Control Register

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TRISx<15:8>[1]							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TRISx<7:0>[1]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **TRISx<15:0>:** PORTx Data Direction Control bits[1]

1 = The pin is an input
0 = The pin is an output

Note 1:   Refer to the specific device data sheet for the actual implementation.

Register 2-2:   PORTx: I/O Portx Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PORTx<15:8>[1]						
bit 15						

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PORTx<7:0>[1]						
bit 7						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **PORTx<15:0>:** I/O Portx bits[1]

1 = The pin data are '1'
0 = The pin data are '0'

Note 1:   Refer to the specific device data sheet for the actual implementation.

Register 2-3:   **LATx: PORTx Data Latch Register**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LATx<15:8>[1]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LATx<7:0>[1]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **LATx<15:0>:** PORTx Data Latch bits[1]

        1 = The latch content is '1'
        0 = The latch content is '0'

Note 1:   Refer to the specific device data sheet for the actual implementation.

Register 2-4:   **ODCx: PORTx Open-Drain Control Register**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ODCx<15:8>[1]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ODCx<7:0>[1]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **ODCx<15:0>:** PORTx Open-Drain Control bits[1]

        1 = The pin acts as an open-drain output pin if TRISx is '0'
   0 = The pin acts as a normal pin

Note 1:   Refer to the specific device data sheet for the actual implementation.

3.0   PERIPHERAL MULTIPLEXING

Pins can also be configured as digital inputs or outputs, and analog inputs or outputs. When configured as digital inputs, they are either TTL buffers or Schmitt Triggers. When configured as digital outputs, they are either CMOS drivers or open-drain outputs.

Many pins also support one or more peripheral modules. When configured to operate with a peripheral, a pin may not be used for general input or output. In many cases, a pin must still be configured for input or output, although some peripherals override the TRIS configuration. Figure 3-1 shows how ports are shared with other peripherals and the associated I/O pin to which they are connected. For some dsPIC33/PIC24 devices, multiple peripheral functions may be multiplexed on each I/O pin. The priority of the peripheral function depends on the order of the pin description in the pin diagram of the specific product data sheet.

Figure 3-1:   Structure of Port Shared with Non-PPS Peripherals

Legend: R = Input buffer type depends on the peripheral. For more information, refer to the specific product data sheet.
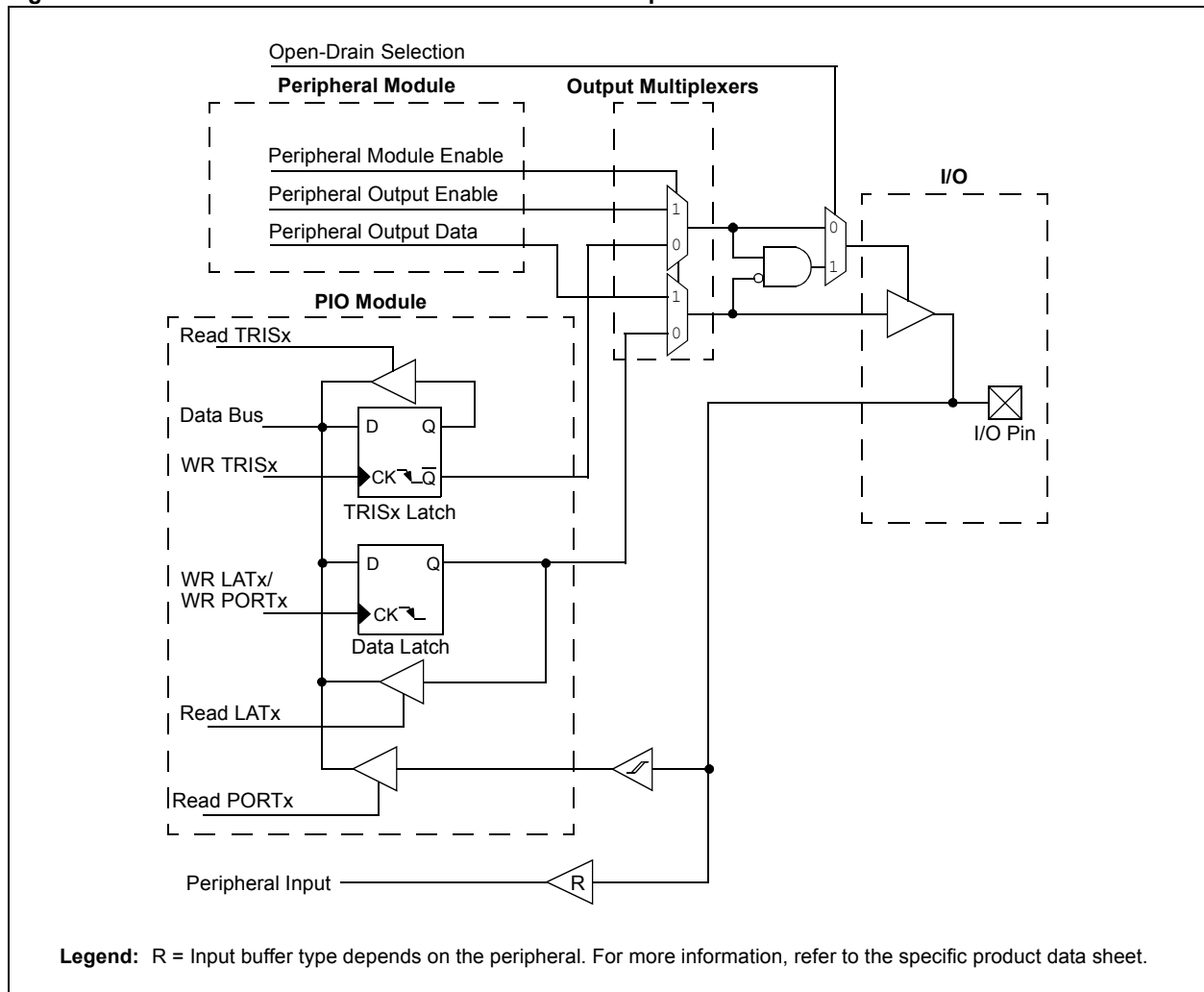
3.1   Multiplexing Digital Input Peripheral

• Peripheral does not control the TRISx register. The TRIS bits should be maintained for input.
• PORTx data input path is unaffected. On reading the PORTx register, the status of the pin will be read.
• Peripheral input path is independent of I/O input path with a special input buffer.

3.2   Multiplexing Digital Output Peripheral

- Peripheral controls output data and PORTx register has no effect.
- PORTx register can read pin value.
- Pad output driver type is selected by peripheral (e.g., drive strength, slow rate, etc.).
- User needs to configure the pin as an output by clearing the associated TRISx bit.
- If an output has an automatic tri-state feature (e.g., PWM outputs), the peripheral has the ability to tri-state the pin.

3.3   Multiplexing Digital Bidirectional Peripheral

- Peripheral can automatically configure the pin as an output but not as an input. User needs to configure the pin as an input by setting the associated TRISx bit.
- Peripherals control output data and PORTx register has no effect.
- PORTx register can read pin value.
- Pad output driver type could be affected by peripheral (e.g., drive strength, slow rate, etc.).

3.4   Multiplexing Analog Input Peripheral

- All digital port input buffers are disabled and PORTx registers read '0' to prevent crowbar current.

3.5   Multiplexing Analog Output Peripheral

- All digital port input buffers are disabled and PORTx registers read '0' to prevent crowbar current.
- Analog output is driven onto the pin independent of the associated TRISx setting.

> **Note:**   In order to use pins multiplexed with the A/D for digital I/O, the corresponding bits in the AD1PCFG register must be set to '1', even if the A/D module is turned off.

3.6   Software Input Pin Control

Some of the functions assigned to an I/O pin may be input functions that do not take control of the pin output driver. An example of one such peripheral is the input capture module. If the I/O pin associated with the input capture is configured as an output, using the appropriate TRIS control bit, the user can manually affect the state of the input capture pin through its corresponding PORT register. This behavior can be useful in some situations, especially for testing purposes, when no external signal is connected to the input pin.

Referring to Figure 3-1, the organization of the peripheral multiplexers will determine if the peripheral input pin can be manipulated in software using the PORT register. The conceptual peripherals shown in this figure disconnect the port data from the I/O pin when the peripheral function is enabled.

In general, the following peripherals allow their input pins to be controlled manually through the PORT registers:

- External Interrupt pins
- Timer Clock Input pins
- Input Capture pins
- PWM Fault pins

Most serial communication peripherals, when enabled, take full control of the I/O pin so that the input pins associated with the peripheral cannot be affected through the corresponding PORT registers. These peripherals include the following:

- SPI
- I^{2}C
- UART

4.0   PERIPHERAL PIN SELECT

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral is needed to be assigned to a single pin, inconvenient work arounds in application code or a complete redesign may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling users peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the microcontroller to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Peripheral Pin Select is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

> **Note:**   Some devices do not have this feature. Please refer to the specific device data sheet for more details.

4.1   Available Pins

The Peripheral Pin Select feature is used with a range of pins. The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the designation, "RPn", in their full pin designation, where "RP" designates a remappable peripheral and "n" is the remappable pin number. If the pin supports only the input function Peripheral Pin Select feature, then it will be designated as "RPIn". For more details, refer to the device pinout in the respective device data sheet.

4.2   Available Peripherals

The peripherals managed by the Peripheral Pin Select are all digital only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and external interrupt inputs.

In comparison, some digital only peripheral modules are not currently included in the Peripheral Pin Select feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I^2C, specialty communication (Ethernet and USB), Change Notification (CN) inputs, RTCC alarm output and all modules with analog inputs, such as the A/D Converter.

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

Figure 4-1: **Structure of Port Shared with PPS Peripherals**
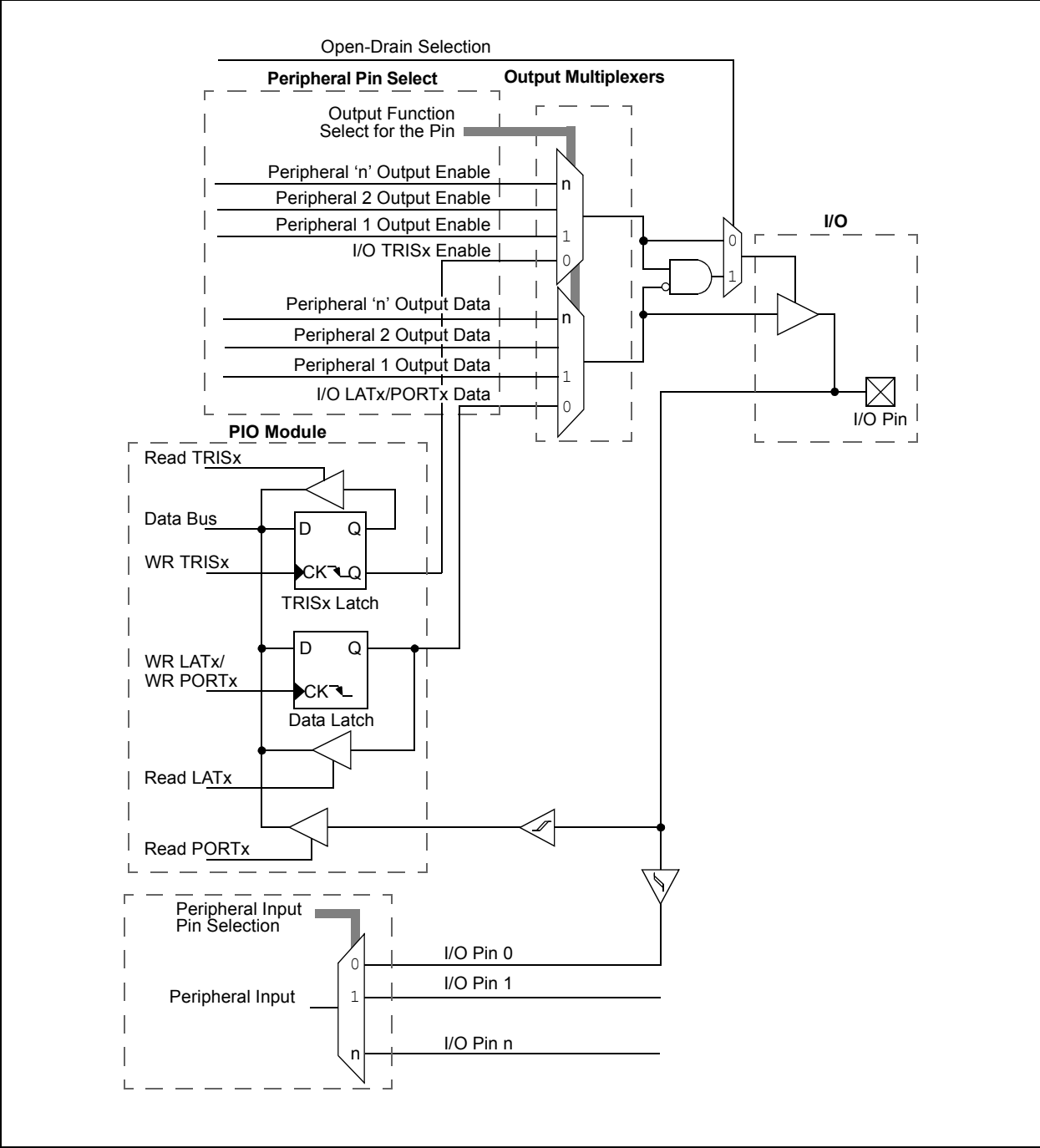
4.3   Controlling Peripheral Pin Select

Peripheral Pin Select features are controlled through two sets of Special Function Registers (SFRs): one to map peripheral inputs and one to map peripheral outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending if an input or output is being mapped.

4.3.1   INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral; that is, a bit field associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers (refer to Register 4-3 and Table 4-1) contain sets of 6-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an RPn value maps the RPn pin to that peripheral. For any given device, the valid range of values for any of the bit fields corresponds to the maximum number of Peripheral Pin Selections supported by the device.

The peripheral inputs that support Peripheral Pin Selection have no default pins. Since the implemented bit fields of RPINRx registers reset to all '1's, the inputs are all tied to Vss in the device's default (Reset) state.

For example, assigning RPINR18<5:0> to 0x2 selects RP2 as the U1RX input. Figure 4-2 illustrates remappable pin selection for the U1RX input.

Figure 4-2:   Remappable Input for U1RX
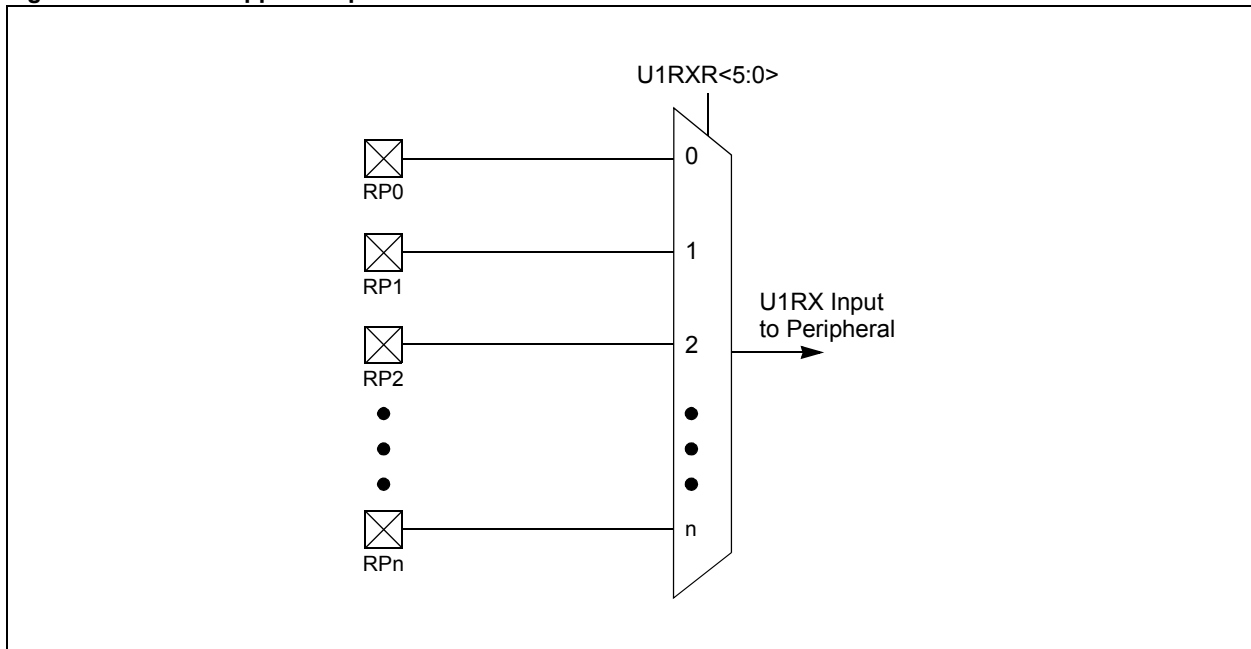
Table 4-1: **Selectable Input Sources (Maps Input to Function)**

Input Name[1]	Function Name	Register Bits	Configuration Bits
External Interrupt 1	INT1	RPINR0<13:8>	INT1R<5:0>
External Interrupt 2	INT2	RPINR1<5:0>	INT2R<5:0>
External Interrupt 3	INT3	RPINR1<13:8>	INT3R<5:0>
External Interrupt 4	INT4	RPINR2<5:0>	INT4R<5:0>
Timer2 External Clock	T2CK	RPINR3<5:0>	T2CKR<5:0>
Timer3 External Clock	T3CK	RPINR3<13:8>	T3CKR<5:0>
Timer4 External Clock	T4CK	RPINR4<5:0>	T4CKR<5:0>
Timer5 External Clock	T5CK	RPINR4<13:8>	T5CKR<5:0>
Input Capture 1	IC1	RPINR7<5:0>	IC1R<5:0>
Input Capture 2	IC2	RPINR7<13:8>	IC2R<5:0>
Input Capture 3	IC3	RPINR8<5:0>	IC3R<5:0>
Input Capture 4	IC4	RPINR8<13:8>	IC4R<5:0>
Input Capture 5	IC5	RPINR9<5:0>	IC5R<5:0>
Output Compare Fault A	OCFA	RPINR11<5:0>	OCFAR<5:0>
Output Compare Fault B	OCFB	RPINR11<13:8>	OCFBR<5:0>
UART1 Receive	U1RX	RPINR18<5:0>	U1RXR<5:0>
UART1 Clear-to-Send	$\overline{U1CTS}$	RPINR18<13:8>	U1CTSR<5:0>
UART2 Receive	U2RX	RPINR19<5:0>	U2RXR<5:0>
UART2 Clear-to-Send	$\overline{U2CTS}$	RPINR19<13:8>	U2CTSR<5:0>
SPI1 Data Input	SDI1	RPINR20<5:0>	SDI1R<5:0>
SPI1 Clock Input	SCK1	RPINR20<13:8>	SCK1R<5:0>
SPI1 Slave Select Input	$\overline{SS1}$	RPINR21<5:0>	SS1R<5:0>
SPI2 Data Input	SDI2	RPINR22<5:0>	SDI2R<5:0>
SPI2 Clock Input	SCK2	RPINR22<13:8>	SCK2R<5:0>
SPI2 Slave Select Input	$\overline{SS2}$	RPINR23<5:0>	SS2R<5:0>

Note 1: The device may have more or less number of input functions. For actual details, please refer to the specific device data sheet.

4.3.2 OUTPUT MAPPING

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a bit field associated with a particular pin dictates the peripheral output to be mapped. The RPORy registers contain sets of 6-bit fields, with each set associated with one RPn pin (see Register 4-4). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 4-1 and Figure 4-3).

The peripheral outputs that support Peripheral Pin Selection have no default pins. Since the RPORy registers reset to all '0's, the outputs are all disconnected in the device's default (Reset) state,

The list of peripherals for output mapping also includes a null value of '000000', because of the mapping technique. This permits any given pin to remain unconnected from the output of any of the pin-selectable peripherals.

Figure 4-3:   Multiplexing of Remappable Output for RPn
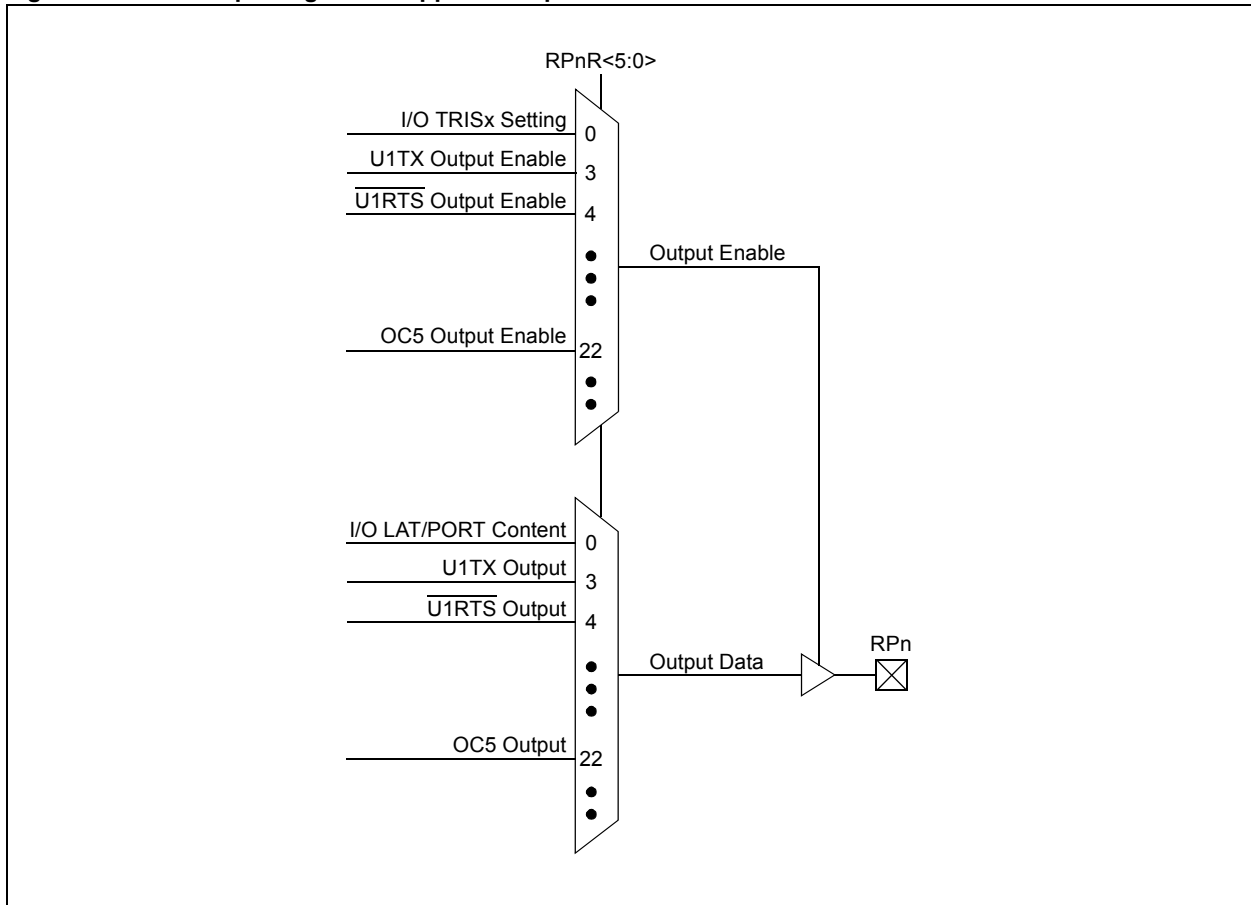
Table 4-1: **Output Selection for Remappable Pin (RPn)**

Function[1]	RPnR<5:0>	Output Name
NULL	0	The pin is an I/O Port pin.
C1OUT	1	RPn tied to Comparator 1 Output.
C2OUT	2	RPn tied to Comparator 2 Output.
U1TX	3	RPn tied to UART1 Transmit.
$\overline{\text{U1RTS}}$	4	RPn tied to UART1 Ready-to-Send.
U2TX	5	RPn tied to UART2 Transmit.
$\overline{\text{U2RTS}}$	6	RPn tied to UART2 Ready-to-Send.
SDO1	7	RPn tied to SPI1 Data Output.
SCK1OUT	8	RPn tied to SPI1 Clock Output.
SS1OUT	9	RPn tied to SPI1 Slave Select Output.
SDO2	10	RPn tied to SPI2 Data Output.
SCK2OUT	11	RPn tied to SPI2 Clock Output.
SS2OUT	12	RPn tied to SPI2 Slave Select Output.
OC1	18	RPn tied to Output Compare 1.
OC2	19	RPn tied to Output Compare 2.
OC3	20	RPn tied to Output Compare 3.
OC4	21	RPn tied to Output Compare 4.
OC5	22	RPn tied to Output Compare 5.

Note 1: The device may have more or less number of output functions. For actual details, please refer to the specific device data sheet.

Table 4-2: **Registers Associated with Output Function on RPn Pin**

Pin	Register	Associated bits
RP0	RPO0<5:0>	RP0R<5:0>
RP1	RPO0<13:8>	RP1R<5:0>
RP2	RPO1<5:0>	RP2R<5:0>
RPn	RPOn/2<5:0>	RPnR<5:0>
RPn + 1	RPOn/2<13:8>	RPn + 1R<5:0>

Legend: n = 0, 2, 4, . . . , etc.

4.3.3 MAPPING LIMITATIONS

The control schema of peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware enforced lockouts between any of the peripheral mapping SFRs; literally any combination of peripheral mappings across any or all of the RPn pins is possible. This includes both many-to-one and one-to-many mappings of peripheral inputs and outputs to pins. While such mappings may be technically possible from a configuration point of view, the user must ensure the selected configurations are supportable from an electrical point of view.

4.4   Controlling Configuration Changes

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. dsPIC33/PIC24 devices include three features to prevent alterations to the peripheral map:

• Control register lock sequence
• Continuous state monitoring
• Configuration bit remapping lock

4.4.1   CONTROL REGISTER LOCK

Under normal operation, writes to the RPINRx and RPORy registers are not allowed; attempted writes will appear to execute normally, but the contents of the registers will remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit (OSCCON<6>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear IOLOCK, a specific command sequence must be executed:

1. Write 46h to OSCCON<7:0>.
2. Write 57h to OSCCON<7:0>.
3. Clear (or set) IOLOCK as a single operation.

The unlock/lock sequence must be executed as an assembly language routine in the same manner as changes to the oscillator configuration, because the unlock sequence is timing critical. If the bulk of the application is written in C, or another high-level language, the unlock sequence should be performed by writing inline assembly or using built-in functions provided by the MPLAB® C30 C Compiler.

IOLOCK remains in one state until changed. This allows all of the Peripheral Pin Selects to be configured with a single unlock sequence, followed by an update to all control registers, then locked with a second lock sequence.

> **Note:**   MPLAB® C Compiler provides built-in C language functions for unlocking the _OSCCON register:
> ```
> __builtin_write_OSCCONL(value)
> __builtin_write_OSCCONH(value)
> ```
> See the *"MPLAB® C Compiler for PIC24 MCUs and dsPIC® DSCs User's Guide"* (www.microchip.com/DS51284) for more information.

4.4.2   CONTINUOUS STATE MONITORING

In addition to being protected from direct writes, the contents of the RPINRx and RPORy registers are constantly monitored in hardware by shadow registers. If an unexpected change in any of the registers occurs (such as cell disturbances caused by ESD or other external events), a Configuration Mismatch Reset (CMR) will be triggered.

4.4.3   CONFIGURATION BIT PIN SELECT LOCK

As an additional level of safety, the device can be configured to prevent more than one write session to the RPINRx and RPORy registers. The IOL1WAY (FOSC<IOL1WAY>) Configuration bit blocks the IOLOCK bit from being cleared after it has been set once.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session. Programming IOL1WAY allows users unlimited access (with the proper use of the unlock sequence) to the Peripheral Pin Select registers.

4.5   Considerations for Peripheral Pin Selection

The ability to control Peripheral Pin Selection introduces several considerations into application design that should be considered.This is particularly true for several common peripherals which are only available as remappable peripherals.

Before any other application code is executed, the user must initialize the device with the proper peripheral configuration. Since the IOLOCK bit resets in the unlocked state, it is not necessary to execute the unlock sequence after the device has come out of Reset. For the sake of application safety, however, it is always a good idea to set IOLOCK and lock the configuration after writing to the control registers.

Choosing the configuration requires the review of all Peripheral Pin Selects and their pin assignments, especially those that will not be used in the application. In all cases, unused pin-selectable peripherals should be disabled. Unused peripherals should have their inputs assigned to Vss. I/O pins with unused RPn functions should be configured with the NULL ('0') peripheral output.

The assignment of an RPn pin to the peripheral input or output depends on the peripheral and its use in the application. It is better to be done immediately following device Reset and before the peripheral configuration.

The assignment of a peripheral output to a particular pin does not automatically perform any other configuration of the pin's I/O circuitry. This means adding a pin-selectable output to a pin may mean inadvertently driving an existing peripheral input when the output is driven. Users must be familiar with the behavior of other fixed peripherals that share a remappable pin. To be safe, fixed digital peripherals that share the same pin should be disabled when not in use.

Configuring a remappable pin for a specific peripheral input does not automatically turn that feature on. The peripheral must be specifically configured for operation and enabled, as if it were tied to a fixed pin.

A final consideration is that Peripheral Pin Select functions neither override analog inputs, nor reconfigure pins with analog functions for digital I/O. If a pin is configured as an analog input on device Reset, it must be explicitly reconfigured as digital I/O when used with a Peripheral Pin Select.

4.5.1   BASIC STEPS TO USE PERIPHERAL PIN SELECTION (PPS)

1. Disable any fixed digital peripherals on the pins to be used.
2. Switch pins to be used for digital functionality (if they have analog functionality) using the ADxPCFG register.
3. Unlock the OSCCON register and clear bit, IOLOCK (not needed after device Reset).
4. Set RPINRx and RPORy registers appropriately.
5. Unlock the OSCCON register and set bit, IOLOCK, to '1'.
6. Configure and enable newly mapped PPS peripherals.

Example 4-1 shows a configuration for bidirectional communication with flow control using UART1. The following input and output functions are used:

• Input Functions: U1RX, $\overline{\text{U1CTS}}$
• Output Functions: U1TX, $\overline{\text{U1RTS}}$

Example 4-1:   Configuring UART1 Input and Output Functions

```
//*****************************************************************
// Unlock Registers
//*****************************************************************
__builtin_write_OSCCONL(OSCCON & 0xbf)   //clear the bit 6 of OSCCONL to
                                         //unlock Pin Re-map
//*********************************************************************
//This code is used when interested in inline assembly. If this code is //
used then the above two lines should not be used for unlocking.
//*********************************************************************
/*
asm volatile    ( "push w1            \n"
                "push   w2            \n"
                "push   w3            \n"
                "mov    #OSCCON, w1   \n"
                "mov    #0x46, w2     \n"
                "mov    #0x57, w3     \n"
                "mov.b  w2, [w1]      \n"
                "mov.b  w3, [w1]      \n"
                "bclr   OSCCON, #6    \n"
                "pop    w3            \n"
                "pop    w2            \n"
                "pop    w1");
*/
//*****************************************************************
// Configure Input Functions
//*****************************************************************
    //***************************
    // Assign U1Rx To Pin RP0
    //***************************
    RPINR18bits.U1RXR = 0;                 //'0' represents RP0

    //***************************
    // Assign U1CTS To Pin RP1
    //***************************
    RPINR18bits.U1CTSR = 1;                //'1' represents RP1

//*****************************************************************
// Configure Output Functions
//*****************************************************************
    //***************************
    // Assign U1Tx To Pin RP2
    //***************************
    RPOR1bits.RP2R = 3;                    //'3' represents U1TX

    //***************************
    // Assign U1RTS To Pin RP3
    //***************************
    RPOR1bits.RP3R = 4;                    //'4' represents U1RTS

//*****************************************************************
// Lock Registers
//*****************************************************************
__builtin_write_OSCCONL(OSCCON | 0x40)   //set the bit 6 of OSCCONL to
                                         //lock Pin Re-map
//*********************************************************************
//This code is used when interested in inline assembly. If this code is //
used then the above two lines should not be used for unlocking.
//*********************************************************************
/*
asm volatile    ( "push w1            \n"
                "push   w2            \n"
                "push   w3            \n"
                "mov    #OSCCON, w1   \n"
                "mov    #0x46, w2     \n"
                "mov    #0x57, w3     \n"
                "mov.b  w2, [w1]      \n"
                "mov.b  w3, [w1]      \n"
                "bset   OSCCON, #6    \n"
                "pop    w3            \n"
                "pop    w2            \n"
                "pop    w1";
*/
```

4.6 Peripheral Pin Select Registers

These registers are used to configure input and output functionality of the dsPIC33/PIC24 device pins.

- **RPINRx:** Peripheral Pin Select Input Register x
- **RPORy:** Peripheral Pin Select Output Register y

Register 4-3: RPINRx: Peripheral Pin Select Input Register x[2]

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	Input Function bits<5:0>[1]					
bit 15							bit 8

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	Input Function bits<5:0>[1]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14   **Unimplemented:** Read as '0'

bit 13-8   **Input Function Bits<5:0>:** Assign Peripheral to Corresponding RPn Pin bits[1]

bit 7-6   **Unimplemented:** Read as '0'

bit 5-0   **Input Function Bits<5:0>** Assign Peripheral to Corresponding RPn Pin bits[1]

Note 1: Here, 'n' represents the peripheral select input pin number.

    2: Here, 'x' represents the Peripheral Pin Select Input register number and it varies from device to device.

Register 4-4: RPORy: Peripheral Pin Select Output Register y[2]

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RPnR<5:0>[1]					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RPnR<5:0>[1]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14   **Unimplemented:** Read as '0'

bit 13-8   **RPnR<5:0>:** Peripheral Output Function is Assigned to RPn Pin bits[1]
(see Table 4-1 for peripheral function numbers)

bit 7-6   **Unimplemented:** Read as '0'

bit 5-0   **RPnR<5:0>:** Peripheral Output Function is Assigned to RPn Pin bits[1]
(see Table 4-1 for peripheral function numbers)

Note 1: Here, 'n' represents the Peripheral Pin Select output pin number.

    2: Here, 'y' represents the Peripheral Pin Select Output register number and it varies from device to device.

5.0 PORT DESCRIPTIONS

Refer to the specific device data sheet for a description of the available I/O ports, peripheral multiplexing details and available Peripheral Pin Select pins.

6.0 CHANGE NOTIFICATION (CN) PINS

The Change Notification (CN) pins provide dsPIC33/PIC24 devices the ability to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. The total number of available CN inputs is dependent on the selected dsPIC33/PIC24 device. Refer to the specific device data sheet for further details.

Figure 6-1 shows the basic function of the CN hardware.

6.1 CN Control Registers

There are four control registers associated with the CN module. The CNENx registers contain the CNxIE control bits, where 'x' denotes the number of the CN input pin. The CNxIE bit must be set for a CN input pin to interrupt the CPU.

The CNPUx/CNPDx registers contain the CNxPUE/CNxPDE control bits. Each CN pin has a weak pull-up/pull-down device connected to the pin, which can be enabled or disabled using the CNxPUE/CNxPDE control bits. The weak pull-up/pull-down devices act as a current source/sink that is connected to the pin and eliminate the need for external resistors when push button or keypad devices are connected. Refer to the **"Electrical Characteristics"** section of the specific device data sheet for CN pull-up/pull-down device current specifications.

Figure 6-1:   **Input Change Notification Block Diagram**
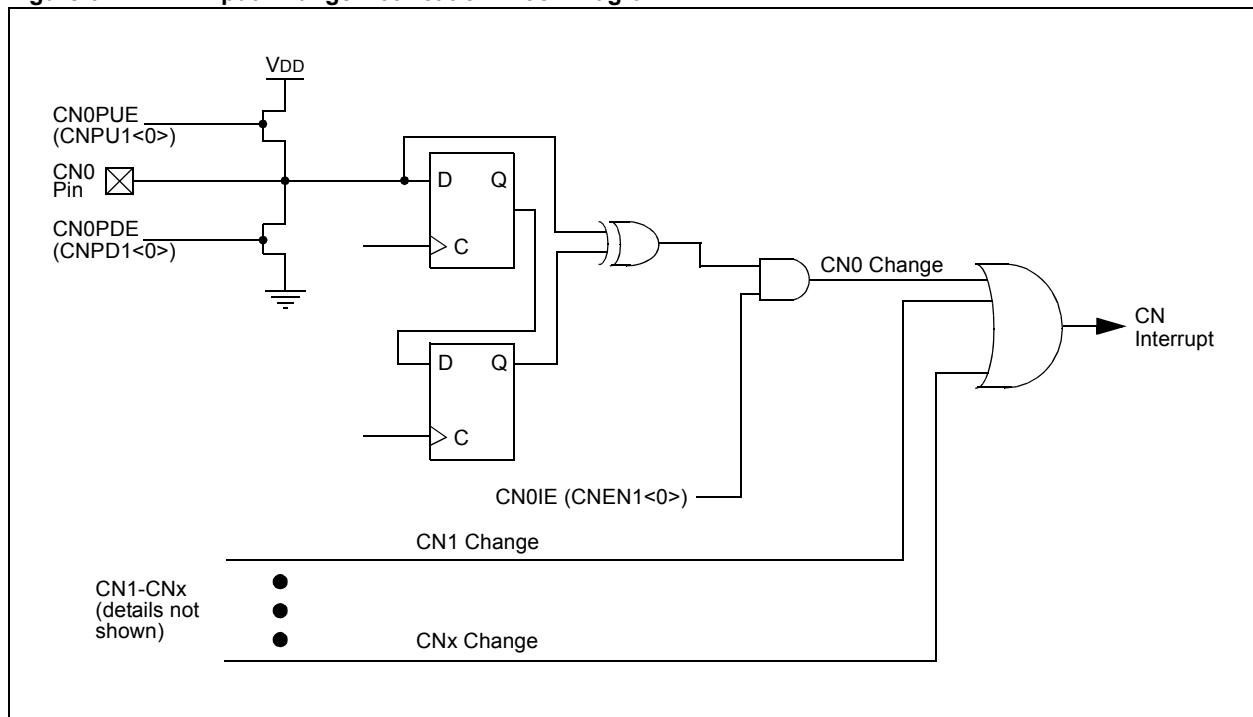
6.2   CN Configuration and Operation

The CN pins are configured as follows:

1. Ensure that the CN pin is configured as a digital input by setting the associated bit in the TRISx register.
2. Enable interrupts for the selected CN pins by setting the appropriate bits in the CNENx registers.
3. Turn on the weak pull-up devices (if desired) for the selected CN pins by setting the appropriate bits in the CNPUx registers.
4. Clear the CNxIF interrupt flag.
5. Select the desired interrupt priority for CN interrupts using the CNxIP<2:0> control bits.
6. Enable CN interrupts using the CNxIE control bit.

When a CN interrupt occurs, the user should read the PORTx register associated with the CN pin(s). This will clear the mismatch condition and set up the CN logic to detect the next pin change. The current PORTx value can be compared to the PORT read value obtained at the last CN interrupt to determine the pin that changed.

The CN pins have a minimum input pulse-width specification. Refer to the **"Electrical Characteristics"** section of the specific device data sheet for further details.

6.3   CN Operation in Sleep and Idle Modes

The CN module continues to operate during Sleep or Idle mode. If one of the enabled CN pins changes states, the CNxIF status bit will be set. If the CNxIE bit is set, the device will wake from Sleep or Idle mode and resume operation.

If the assigned priority level of the CN interrupt is equal to, or less than, the current CPU priority level, device execution will continue from the instruction immediately following the SLEEP or IDLE instruction.

If the assigned priority level of the CN interrupt is greater than the current CPU priority level, device execution will continue from the CN interrupt vector address.

7.0 REGISTER MAPS

A summary of the registers associated with the dsPIC33/PIC24 I/O ports is provided in Table 7-1, Table 7-2 and Table 7-3.

Table 7-1: Special Function Registers Associated with I/O Ports[1]

Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISx	PORTx Data Direction Control bits																FFFF
LATx	PORTx Data Latch bits																xxxx
PORTx	Rx15	Rx14	Rx13	Rx12	Rx11	Rx10	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	Rx1	Rx0	xxxx
ODCx	PORTx Open-Drain Control bits																0000

Note 1: Refer to the specific device data sheet for the I/O Ports register map details.

Table 7-2: Special Function Registers Associated with Peripheral Pin Selection[1]

Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINRx	—	—	Input Function bits<5:0>						—	—	Input Function bits<5:0>						3F3F[2]
RPORy	—	—	RPnR<5:0>						—	—	RPnR<5:0>						0000

Note 1: Refer to the specific device data sheet for Peripheral Pin Select register map details.

2: The number of bits implemented varies with the number of pins the device has.

Table 7-3: Special Function Registers Associated with Change Notification Pins[1]

Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNENx	Change Notification Interrupt Enable bits																0000
CNPUx	Change Notification Pull-up Enable bits																0000
CNPDx	Change Notification Pull-Down Enable bits																0000

Note 1: Refer to the specific device data sheet for Change Notification Pin register details.

8.0   RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33/PIC24 families of devices, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the I/O Ports with Peripheral Pin Select (PPS) are:

Title	Application Note #
Implementing Wake-up on Key Stroke	AN552

> **Note:**   Please visit the Microchip website (www.microchip.com) for additional application notes and code examples for the dsPIC33/PIC24 families of devices.

9.0 REVISION HISTORY

Revision A (August 2006)

This is the initial released revision of this document.

Revision B (May 2007)

Added PPS section, removed JTAG boundary scan section and added PPS SFR table.

Revision C (March 2019)

Updated the reference manual to the latest template format.

Added a note to **Section 2.1 "TRIS Registers"**.

NOTES:

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