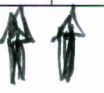
PIC24FV32KA304 FAMILY

PIC24F Device	Pins	Memory			Timers 16-Bit	Capture Input	Compare/PWM Output	UART w/ IrDA®	SPI	I²C™	12-Bit A/D (ch)	Comparators	CTMU (ch)	RTCC
		Flash Program (bytes)	SRAM (bytes)	EE Data (bytes)										
PIC24FV16KA301 /PIC24F16KA301	20	16K	2K	512	5	3	3	2	2	2	12	3	12	Y
PIC24FV32KA301 /PIC24F32KA301	20	32K	2K	512	5	3	3	2	2	2	12	3	12	Y
PIC24FV16KA302 /PIC24F16KA302	28	16K	2K	512	5	3	3	2	2	2	13	3	13	Y
PIC24FV32KA302 /PIC24F32KA302	28	32K	2K	512	5	3	3	2	2	2	13	3	13	Y
PIC24FV16KA304 /PIC24F16KA304	44	16K	2K	512	5	3	3	2	2	2	16	3	16	Y
PIC24FV32KA304 /PIC24F32KA304	44	32K	2K	512	5	3	3	2	2	2	16	3	16	Y



INPUT CAPTURE

14.0 INPUT CAPTURE WITH DEDICATED TIMERS

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"PIC24F Family Reference Manual"*, **Section 34. "Input Capture with Dedicated Timer"** (DS39722).

All devices in the PIC24FV32KA304 family features 3 independent input capture modules. Each of the modules offers a wide range of configuration and operating options for capturing external pulse events and generating interrupts.

Key features of the input capture module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 20 user-selectable trigger/sync sources available
- A 4-level FIFO buffer for capturing and holding timer values for several events
- Configurable interrupt generation
- Up to 6 clock sources available for each module, driving a separate internal 16-bit counter

The module is controlled through two registers: ICxCON1 (Register 14-1) and ICxCON2 (Register 14-2). A general block diagram of the module is shown in Figure 14-1.

14.1 General Operating Modes

14.1.1 SYNCHRONOUS AND TRIGGER MODES

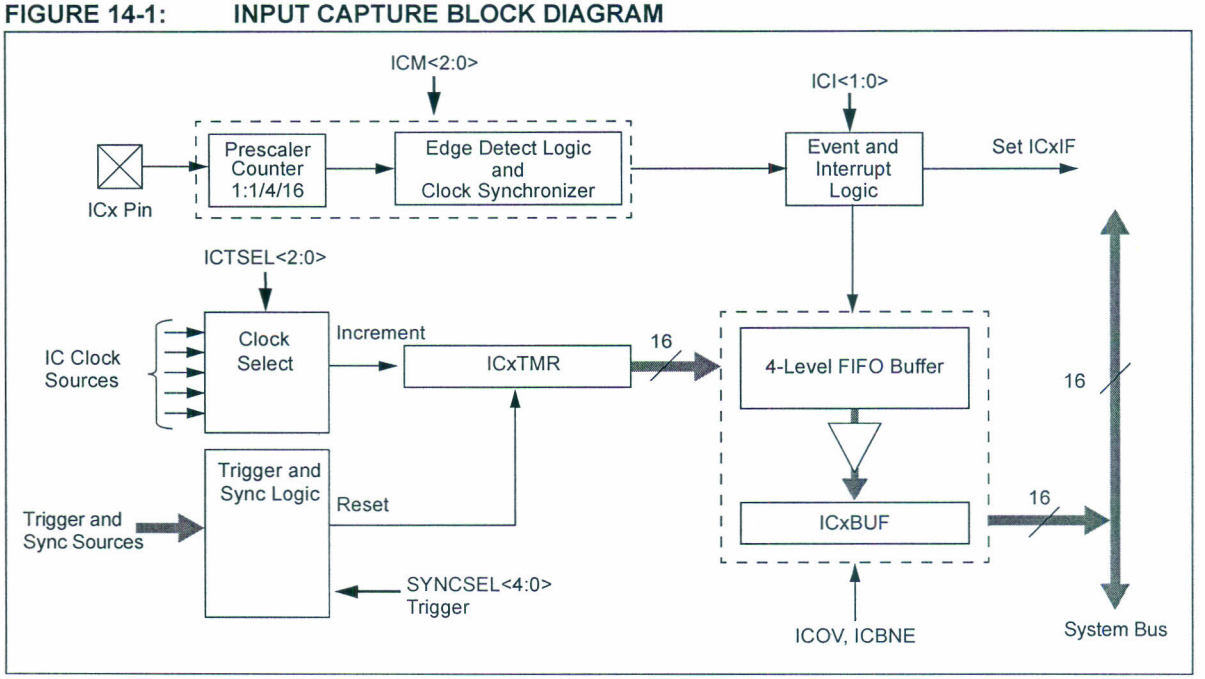
By default, the input capture module operates in a free-running mode. The internal 16-bit counter, ICxTMR, counts up continuously, wrapping around from FFFFh to 0000h on each overflow, with its period synchronized to the selected external clock source. When a capture event occurs, the current 16-bit value of the internal counter is written to the FIFO buffer.

In Synchronous mode, the module begins capturing events on the ICx pin as soon as its selected clock source is enabled. Whenever an event occurs on the selected sync source, the internal counter is reset. In Trigger mode, the module waits for a Sync event from another internal module to occur before allowing the internal counter to run.

Standard, free-running operation is selected by setting the SYNCSEL bits to '00000' and clearing the ICTRIG bit (ICxCON2<7>). Synchronous and Trigger modes are selected any time the SYNCSEL bits are set to any value except '00000'. The ICTRIG bit selects either Synchronous or Trigger mode; setting the bit selects Trigger mode operation. In both modes, the SYNCSEL bits determine the sync/trigger source.

When the SYNCSEL bits are set to '00000' and ICTRIG is set, the module operates in Software Trigger mode. In this case, capture operations are started by manually setting the TRIGSTAT bit (ICxCON2<6>).

FIGURE 14-1: INPUT CAPTURE BLOCK DIAGRAM



CAPTURE

1. DETERMINE TIME OF SWITCH CLOSURE (OR LOGIC TRANSITION)

   a. SET UP CAPTURE AND TIMER1 WITH INTERRUPT

   b. READ COUNT AFTER EVENT

2. CAPTURE PULSE WIDTH (PEATMAN PLOT)

   a) CAPTURE TIME OF RISING EDGE

   b) CLEAR INTERRUPT FLAG AND DISABLE INTERRUPTS (11:3.3 in Data sheet)

   c) SET UP CAPTURE ON FALLING EDGE

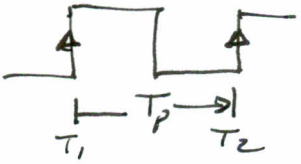
$T_2 - T_1$ = WIDTH

NOTE: $T_2 - T_1$ MUST BE LONG ENOUGH TO CHANGE CAPTURE MODE! AFTER INTERRUPT (b above) IS SERVICED.

INPUT CAPTURE

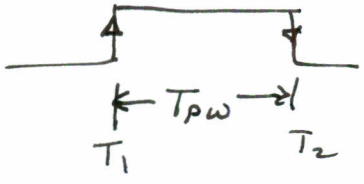
- INTERRUPT ON CHANGE OF STATE OF INPUT

- PERIOD MEASUREMENT



$T_P = T_2 - T_1$

- PULSE WIDTH



$T_{PW} = T_2 - T_1$

NOTE: 1. T_P OR T_{PW} SHOULD BE LESS THAN THE TIME RANGE OF THE COUNTER – UNLESS OVERFLOWS ARE COUNTED

2. THE ACCURACY WILL DEPEND ON THE RESOLUTION OF THE TIMER $\frac{1}{f_{TIMER\ CLOCK}}$

IN PRACTICE, THE PULSE WIDTH COULD BE PROPORTIONAL TO ALMOST ANY VALUE (RESISTANCE, TEMPERATURE, ETC.)

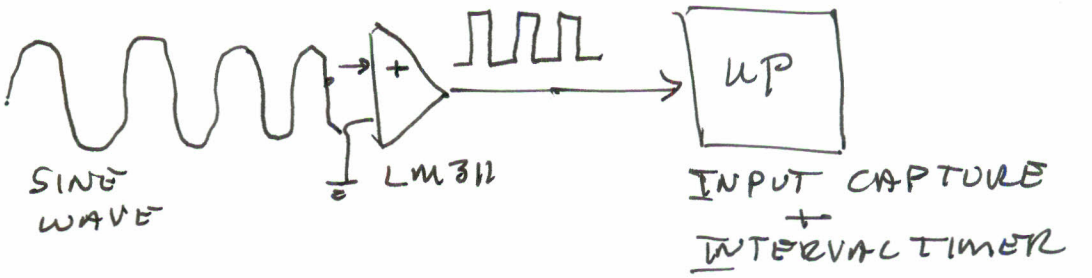
8 bit TIMER/COUNTER $T_{CLKT_1} = 10^{-3}$ s

RESOLUTION ~ 1ms

RANGE ~ $(2^8 - 1)$ 1ms = 255ms

EXAMPLES

FREQUENCY MEASUREMENT —
COUNT PULSES



$$f = \frac{\text{COUNTER}}{\text{FIXED TIME}} \quad (Hz)$$

$$\Delta f = \frac{1}{\text{FIXED TIME}} \; Hz \qquad \text{RESOLUTION}$$

i.e 5 PULSES IN 10 ms $\quad f = \frac{5}{10 \times 10^{-3}} = 500 Hz$

period = 2 ms